

U.S. Patent Application Serial No. 09/855,590

the lower metal wiring layer M1 having a width W1 and an upper metal wiring layer M4 having a width W4 intersect with the intermediate metal layers M2 and M3 sandwiched in between. In this example, SVIA that have been placed in an array configuration matching the wiring tracks in the priority wiring direction of the intermediate metal layers M2 and M3 over the entire surface of the intersection portion 10 are deleted in line units.

Please replace the paragraph beginning at page 10, line 22 with the following rewritten paragraph:

Specifically, an example is given of when it is possible to delete one row in the X direction and two rows in the Y direction for a total of nine SVIAs, when five rows of SVIA are arranged at the pitch PX in the X direction (i.e., in the transverse direction of the upper metal wiring layer M4) and three rows of SVIA are arranged at the pitch PY in the Y direction (i.e., in the transverse direction of the lower metal wiring layer M1) for a total of fifteen SVIAs. As a result, it is possible to secure one wiring track L3 through which wiring is able to pass from among the three wiring tracks T3 in the X direction and two wiring tracks L2 through which wiring is able to pass from among the five wiring tracks T2 in the Y direction.

IN THE CLAIMS:

Cancel claim 17.

Amend claims 1 and 2 as follows: